



PTO/SB/08a (07-05)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1

of 2

Complete if Known

Application Number	10/770,435
Filing Date	February 3, 2004
First Named Inventor	Shi
Art Unit	2816
Examiner Name	Luu, A.
Attorney Docket Number	RAMB-01015US1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
AZ		US-6504438	01-07-2003	Chang et al.	
AZ		US-6809600 B2	10-26-2004	Chang et al.	
AZ		US-6928128 B1	08-09-2005	Sidiropoulos	
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FOREIGN PATENT DOCUMENTS

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Examiner Name

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Attorney Docket Number

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
KU		CHANG et al., "A 0.4-4Gb/s CMOS Quad Transceiver Cell using On-chip Regulated Dual-Loop PLLS," 2002 Symposium on VLSI Circuits Digest of Technical Papers	
KU		SIDIROPOULOS et al., "A Semidigital Dual Delay-Locked Loop," IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997	
KU		MANEATIS, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996	

Examiner Signature	Luu	Date Considered	8/1/06
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NON PATENT LITERATURE DOCUMENTS

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A2U		SIDIROPOULOS et al., "Adaptive Bandwidth DLLs and PLLs using Regulated Supply CMOS Buffers," 2000 Symposium on VLSI Circuits Digest of Technical Papers, 2000 IEEE	

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